Electrical Degradation of InAlN/GaN HEMTs Operating Under ON Conditions

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***Abstract*— The degradation of InAlN/GaN high-electron-mobility transistors (HEMTs) for millimeter-wave applications has been examined under on conditions. Two dominant permanent degradation mechanisms have been identified as well as two trapping mechanisms which affect the device characteristics in different ways. Under high-voltage, low-current stress conditions, we have observed permanent enhancement in the maximum drain current $I_{D\max}$ that arises from a negative shift in threshold voltage V_T. We attribute this mechanism to depassivation of hydrogenated defects. Under the same stress conditions, there is prominent and reversible hot-electron trapping on the drain side of the device that brings $I_{D\max}$ down and increases the drain resistance. Under low-voltage high-current stress conditions, there is a visible permanent reduction in $I_{D\max}$ and a positive shift in V_T. This is also the signature of-high temperature stress under unbiased conditions and is attributed to gate sinking.**

***Index Terms*— Gate sinking, InAlN/GaN, threshold voltage, trapping.**

I. Introduction

FIRST demonstrated in the 1990s, AlGaN/GaN HEMTs for high-frequency power amplifier applications have recently become commercially available. In the quest for enhancing the operating frequency of GaN HEMTs, there has been a great effort to scale the gate length. Maintaining acceptable short-channel effects requires shrinking the gate barrier. A limitation exists to this since there is a minimum barrier thickness that is needed to obtain a sufficiently large 2-D electron gas (2-DEG) density. A solution to this problem is the use of a new barrier layer material, i.e., InAlN [1].

Due to its high spontaneous polarization, a much smaller thickness of InAlN as barrier layer in InAlN/GaN HEMTs is required in order to achieve high enough 2-DEG density, compared with AlGaN. This enables barrier thickness scaling and therefore gate length scaling. Furthermore, with $x = 17\%$, $In_{0.17}Al_{0.83}N$ can be grown lattice matched to GaN. This confers InAlN/GaN HEMTs with potentially better reliability. Recently, InAlN/GaN E-mode and D-mode HEMTs with $f_T/f_{\max} > 300$ GHz have been reported [2]. Also, InAlN/AlN/GaN MIS-HEMTs with simultaneous high breakdown voltage and high f_T have been realized [3]. In addition, there has been the successful demonstration of InAlN/GaN HEMTs on Si with a high Johnson figure-of-merit (FOM) of 101 GHz [4].

Despite all the promising properties of this novel heterostructure system, problems exist that require further research. Among them, the relatively less mature growth technique for InAlN brings new reliability concerns. Unfortunately, in this regard, the literature is very sparse. It has been reported that indium concentration variations during InAlN epitaxy growth can lead to excessive gate leakage current in InAlN/GaN HEMTs [5]–[9]. Also, with extremely scaled gate stacks, the electric field across the gate and channel can become much larger than in AlGaN/GaN HEMTs, suggesting that hot-electron degradation could be a serious concern [10]–[14].

This manuscript presents a study of reliability issues in InAlN/GaN HEMTs with emphasis on the ON regime at high $V_{D\text{stress}}$. Previous studies [15] under similar conditions did not make an effort to control for device self-heating. In our work, by conducting constant-power-stress experiments with varying $V_{D\text{stress}}$ and $I_{D\text{stress}}$, we are able to isolate the impact of self-heating. This has allowed us to identify two separate permanent degradation mechanisms as well as two different trapping mechanisms.

II. Methodology and Initial Electrical Reliability Survey

The devices used in this study are W-band InAlN/GaN HEMTs fabricated by our industrial collaborator. The heterostructure consists of a 5-nm InAlN barrier layer, a 1-nm AlN interfacial layer, and an unintentionally doped GaN channel. The heterostructure was grown by MOCVD. In the device fabrication, the InAlN barrier is recessed so that the gate metal stack, consisting of Ni/Au, is directly placed on top of the AlN interfacial layer. This yields a positive threshold voltage. The transistors feature a gate length $L_g = 40$ nm and gate width W_g ranging from 50 to 400 μm. L_{gd} and L_{gs} are both 1 μm. The intended operating voltage for the devices is 15 V. All stress and characterization measurements were conducted with an Agilent B1500A semiconductor parameter analyzer.

An initial survey of the electrical reliability of these devices was performed under OFF-state, semi-ON-state, and ON-state conditions. In order to be able to separate permanent from trap-related device degradation, we developed a benign detrapping technique that consisted of a thermal annealing step at 100 °C

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TABLE I

CHANGES OF $I_{D\max}$ (I_D AT V_{DS} = 5 V, V_{GS} = 2 V), V_{Tlin} (V_{GS} AT I_D = 1 mA/mm WITH V_{DS} = 0.1 V), R_D, AND R_S (MEASURED WITH AN INJECTED CURRENT OF 20 mA/mm FROM GATE [20]) WITH RESPECT TO THE VIRGIN STATE AFTER DELIBERATELY INTRODUCING TRAPPING (SEE TEXT) AND AFTER THERMAL DETRAPPING

	$\Delta I_{Dmax}/I_{Dmax}(0)$ [%]	V_{Tlin}-$V_{Tlin}(0)$ [mV]	$R_D/R_D(0)$	$R_S/R_S(0)$
Initial	0	0	1	1
After trapping	0.70	-23.4	0.95	0.89
After detrapping	0.00	2.3	1.01	1.00

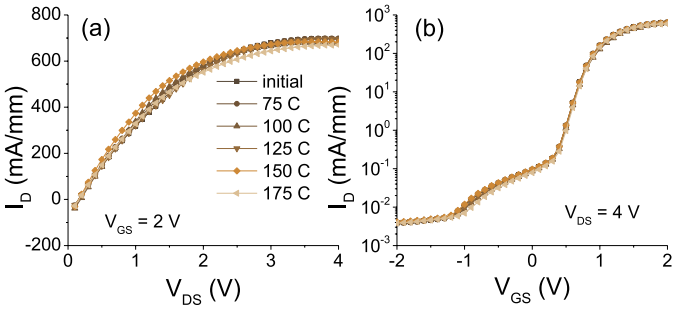

Fig. 1. (a) Output (V_{GS} = 2 V) and (b) transfer characteristics (V_{DS} = 4 V) after OFF-state stress with T_{stress} ranging from 75 °C to 175 °C. Device characterization was conducted at 25 °C after thermal detrapping. Negligible permanent degradation takes place as a result of the entire stress experiment.

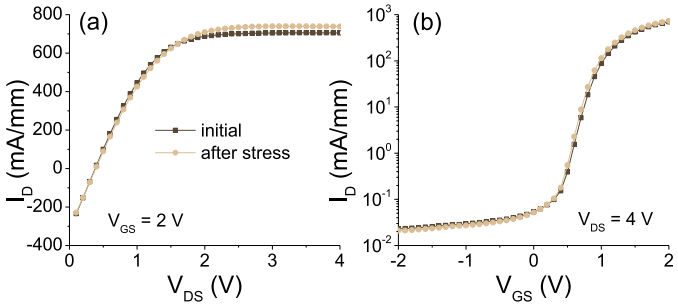

Fig. 2. (a) Output (V_{GS} = 2 V) and (b) transfer characteristics (V_{DS} = 4 V) before and after semi-ON-state stress (V_{GS} = 0.5 V) followed by a detrapping step. Negligible permanent degradation happens.

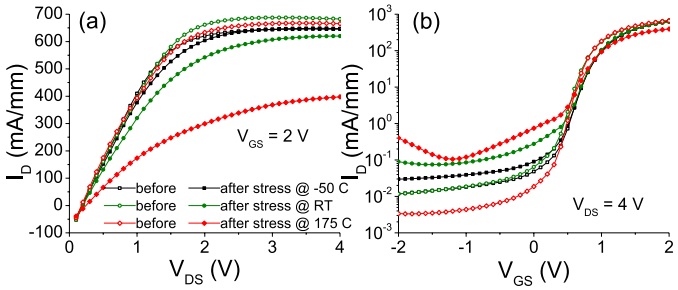

Fig. 3. (a) Output (V_{GS} = 2 V) and (b) transfer characteristics (V_{DS} = 4 V) after ON-state step stress (V_{GS} = 1.5 V) at −50 °C, RT, and 175 °C, measured at 25 °C after thermal detrapping. Significant saturation drain current decrease, leakage current increase, and positive threshold voltage shift are observed. Also, strong temperature-accelerated permanent degradation becomes evident.

for 1 h. This detrapping approach was verified to be benign and effective in recovering the device characteristics by comparing the change in selected FOMs of a virgin device after deliberately introducing trapping and after the thermal anneal step. Table I shows the change of $I_{D\max}$, $V_{T\lin}$, R_D, and R_S after repeated I_D–V_{DS} and I_D–V_{GS} sweeps (200 times) to introduce trapping. We can see that all FOMs completely recover (within the resolution of our instrumentation) after device baking. In all our electrical stress experiments, we initialize the virgin devices by performing this thermal annealing step to create a stable reference point with which we compare further changes.

Electrical stress experiments have been conducted under OFF-state (Fig. 1) with V_{DS} stepping up from 5 to 40 V in 5 V step at V_{GS} = −2 V. Experiments were repeated at different temperatures starting from T_{stress} = 75 °C and ending at 175 °C in steps of 25 °C. For each chosen T_{stress} value, the device was stressed at each V_{DS} level for 5 min and was characterized every 1 min during stress. After a sequence of experiments at a given temperature and before moving over to the next temperature, the device was completely detrapped and a complete set of I–V sweeps was obtained. As seen in Fig. 1, negligible permanent degradation took place as a result of the entire sequence of OFF-state stress in this experiment. This presents a significant improvement upon AlGaN/GaN HEMTs where a critical voltage of less than 40 V has often been observed [16]. This can be due to the absence of lattice-mismatch-induced tensile strain, which allows InAlN/GaN to be able to withstand a higher gate-drain electric field.

Semi-ON-state stress experiments were also performed. In these, V_{DS} was stepped up from 5 to 40 V in 5 V steps at V_{GS} = 0.5 V (I_D ∼ 10 mA/mm) at room temperature (RT). Each step was held for 5 min and the device was characterized every 1 min. As Fig. 2 shows, negligible permanent degradation was observed. This is similar to what has been reported before in this material system [14], [17]–[19].

ON-state stress experiments were also carried out at −50 °C, RT, and 175 °C on three different devices with V_{DS} stepping up from 0 to 40 V in 1 V steps at V_{GS} = 1.5 V (I_D ∼ 400 mA/mm). Under these harsh conditions, we observed strong temperature-accelerated permanent degradation as reflected mainly by a significant $I_{D\max}$ decrease and a positive V_T shift (Fig. 3).

Based on these early experiments in which ON-state stress emerged as a problematic regime, we decided to study ON-state degradation in more detail. To avoid complications due to device self-heating, we designed a series of constant-power stress experiments that are described in the following section.

III. CONSTANT-POWER STRESS EXPERIMENTS

We carried out electrical stress experiments under constant power conditions in which $V_{D\text{stress}}$ was progressively increased while $I_{D\text{stress}}$ was decreased such that the $V_{D\text{stress}} \times I_{D\text{stress}}$ product was maintained constant. Under the assumption that

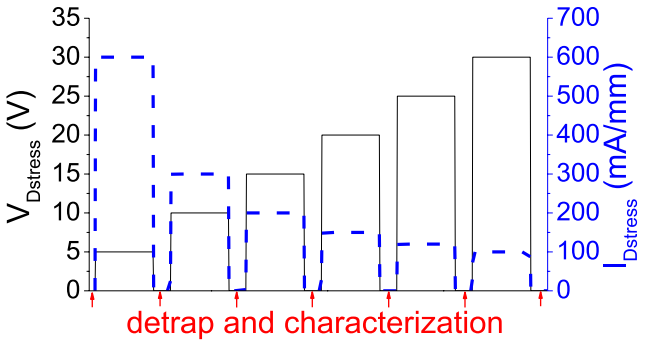

Fig. 4. Evolution of stress conditions and characterization during constant-power stress experiments. Stress time for each ($V_{D\text{stress}}$, $I_{D\text{stress}}$) level is 10 min and detrapping is conducted at the end of each level by baking the DUT at 100 °C for 1 h. Time evolves from left to right in two experiments and from right to left in a third one.

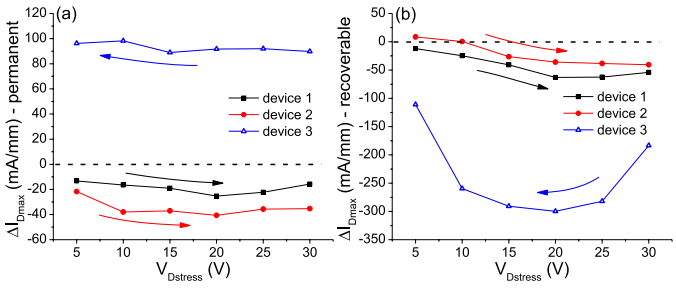

Fig. 5. (a) Permanent $I_{D\max}$ degradation [defined as $\Delta I_{D\max} = (I_{D\max} - I_{D\max}(0)]$ and (b) recoverable $I_{D\max}$ degradation as a function of stress voltage, $V_{D\text{stress}}$. Black (device 1) and red marks (device 2) correspond to the two experiments with increasing $V_{D\text{stress}}$ and blue marks (device 3) correspond to the experiment with decreasing $V_{D\text{stress}}$.

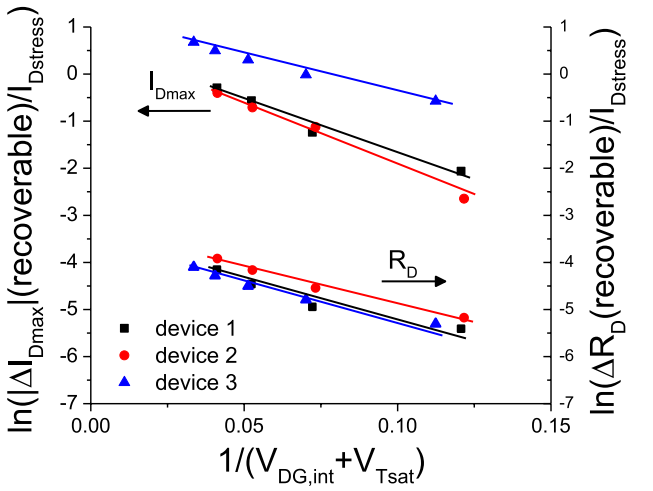

Fig. 6. Hot-electron type plots of recoverable $|\Delta I_{D\max}|$ and R_D in the three constant-power stress experiments.

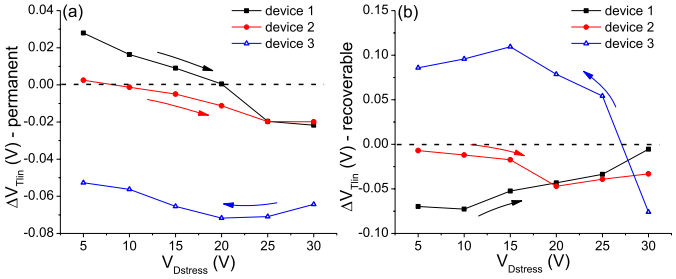

Fig. 7. (a) Permanent and (b) recoverable change in $V_{T\text{lin}}$ as a function of stress voltage $V_{D\text{stress}}$. Black (device 1) and red (device 2) marks represent the two experiments with increasing $V_{D\text{stress}}$ levels, while blue marks (device 3) represent the experiment with decreasing $V_{D\text{stress}}$ levels.

device self-heating is proportional to the dissipated power, the junction temperature in these experiments should be relatively unchanged. By varying $V_{D\text{stress}}$ and $I_{D\text{stress}}$, we should then be able to separately identify the effect of high voltage and high current on device reliability.

Fig. 4 shows the experiment sequence. $V_{D\text{stress}}$ is increased from 5 to 30 V in 5 V steps while $I_{D\text{stress}}$ is decreased from 600 to 100 mA/mm, keeping $V_{D\text{stress}} \times I_{D\text{stress}}$ constant at 3 W/mm. Using the thermal model provided by our industrial collaborator, the estimated junction temperature under this condition is around 65 °C. The device was stressed for 10 min at each level. It was then detrapped and characterized before moving to the next stress level. Two experiments were carried with time running from left to right (increasing $V_{D\text{stress}}$ and decreasing $I_{D\text{stress}}$), while one more was performed with time running from right to left (decreasing $V_{D\text{stress}}$ and increasing $I_{D\text{stress}}$).

The typical results from the three experiments are shown in Fig. 5. The arrows in the graphs indicate the direction of time evolution during the experiments. The x-axes graph $V_{D\text{stress}}$ and the y-axes graph permanent I_D degradation [Fig. 5(a)] and recoverable I_D degradation [Fig. 5(b)] accumulated at each step were measured with respect to the initial value $I_{D\max}$ (0). Permanent $I_{D\max}$ degradation is defined as the change in $I_{D\max}$ after device detrapping, which was done after each stress step. Recoverable $I_{D\max}$ is the overall $I_{D\max}$ change minus the permanent component.

In both devices 1 and 2, the majority of permanent $I_{D\max}$ drop happens at relatively low $V_{D\text{stress}}$ with little additional degradation taking place at higher $V_{D\text{stress}}$. In particular, for device 2, there is no further degradation in permanent $I_{D\max}$ after $V_{D\text{stress}} = 10$ V. Beyond a value of $V_{D\text{stress}}$ of around 20 V, we see a small apparent recovery of permanent $I_{D\max}$ that is enhanced as $V_{D\text{stress}}$ increases.

In addition to the permanent change in $I_{D\max}$, for devices 1 and 2, there is a recoverable $I_{D\max}$ drop that worsens as $V_{D\text{stress}}$ increases. This reflects increased trapping. We have analyzed this drop in recoverable $I_{D\max}$ and found that it follows a hot electron-type law [21]. This is shown in Fig. 6,which graphs the logarithmic of recoverable $|\Delta I_{D\,\max}|/I_{D\text{stress}}$ versus $1/(V_{\text{DG,int}} + V_{T\text{sat}})$. Here $V_{\text{DG,int}}$ is the intrinsic portion of the gate-drain voltage, which properly excludes the voltage drop in the device extrinsic regions due to R_D and R_S. $V_{T\text{sat}}$ is the threshold voltage extracted at $V_{\text{DS}} = 4$ V as the linear extrapolation of I_D–V_{GS} curve at peak g_m to zero current.

The clear linear dependence that emerges in Fig. 6 once $V_{\text{DG,int}}$ is large enough indicates that the recoverable drain current degradation in these devices depends exponentially on the electric field in the gate-drain intrinsic region and linearly on the channel current during stress. This suggests that this

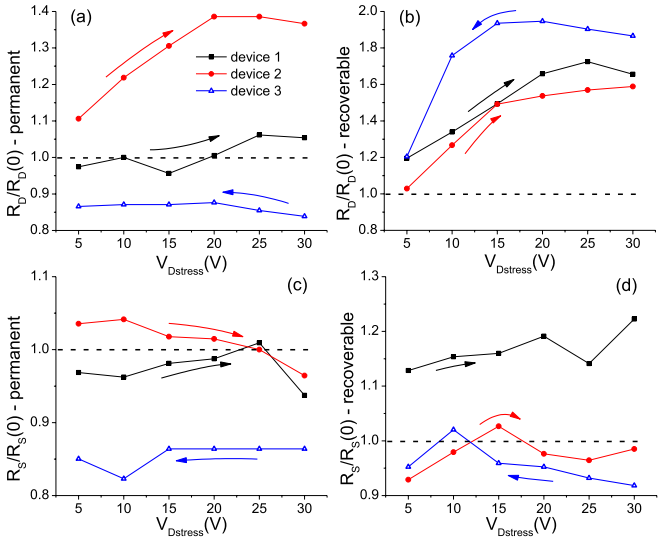

Fig. 8. (a) Permanent, (b) recoverable R_D degradation and (c) permanent, (d) recoverable R_S degradation as a function of bias voltage applied on the drain $V_{D\text{stress}}$. Black (device 1) and red marks (device 2) correspond to the two experiments with increasing $V_{D\text{stress}}$ and blue marks (device 3) correspond to the experiment with decreasing $V_{D\text{stress}}$.

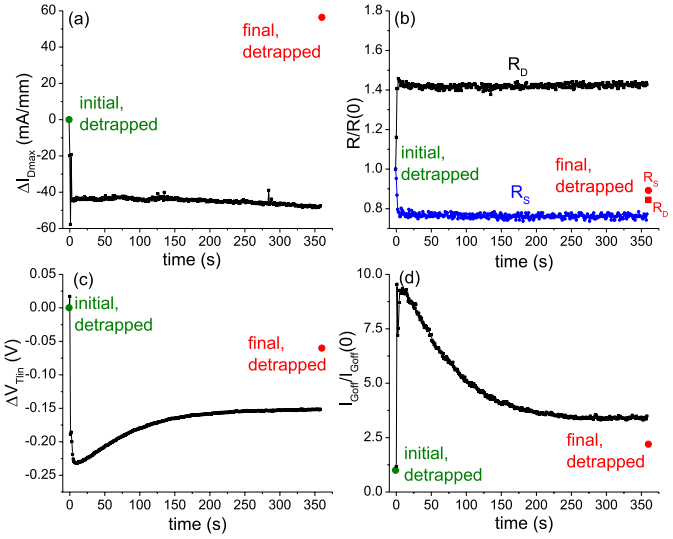

Fig. 9. Evolution of (a) $\Delta I_{D\text{max}}$, (b) R_D, R_S, (c) $\Delta V_{T\text{lin}}$, and (d) $I_{\text{Goff}}/I_{\text{Goff}}$ (0) during constant high-V_D–low-I_D stress. Initial and final detrapped values are also given.

degradation mechanism is due to trapping of hot electrons on the drain side of the device inside the InAlN layer or at its interface with the passivation layer above.

In order to further understand the results in Fig. 5, Fig. 7 shows the change in $V_{T\text{lin}}$ (obtained from the linear extrapolation of I_D from the peak g_m point to 0 at $V_{\text{DS}} = 0.1$ V), both permanent and recoverable. As a result of stress, there is an initial relatively small positive shift in the permanent $V_{T\text{lin}}$ that then drops and eventually turns negative. In addition, there is a negative recoverable change in $V_{T\text{lin}}$ that is less consistent in its behavior. The negative shift in permanent V_T as $V_{D\text{stress}}$ increases explains the apparent recovery of permanent $I_{D\text{max}}$ degradation under the same conditions that were observed in Fig. 5(a). Changes in the source and drain resistances largely confirm this picture. As shown in Fig. 8(a), permanent degradation in R_D tends to increase in the early stages under low $V_{D\text{stress}}$. Relative to this, the changes in the source resistance [Fig. 8(c)] are smaller. These results suggest that the $V_{D\text{stress}}$-enhanced permanent damage takes place on the drain side of the device. The recoverable component of R_D degradation [Fig. 8(b)] also follows a hot-electron type law (Fig. 6), while the recoverable change in R_S [Fig. 8(d)] is small. This further confirms high-electric field-induced hot-electron trapping on the drain side.

In order to bring a new perspective and understand the small apparent recovery of permanent $I_{D\text{max}}$ that is enhanced at high $V_{D\text{stress}}$, we conducted a similar constant-power-stress experiment with $V_{D\text{stress}}$ this time starting fresh from 30 V and decreasing to 5 V in 5 V steps, while keeping $V_{D\text{stress}} \times I_{D\text{stress}}$ fixed at 3 W/mm as before. The results are also shown in Figs. 5–8 (blue marks, device 3). The new experiment reveals a permanent *increase* instead of a decrease in drain current with the majority of this increase happening at $V_{\text{Dstress}} = 30$ V [Fig. 5(a)]. There is also prominent recoverable degradation of $I_{D\text{max}}$ that again follows a hot-electron type law [Figs. 5(b) and 6, blue marks] consistent with the earlier experiments. At the same time, high $V_{D\text{stress}}$ results in a permanent negative V_T shift that remains relatively stable as $V_{D\text{stress}}$ is reduced [Fig. 7(a)]. This is also consistent with the behavior of permanent $I_{D\text{max}}$ in Fig. 5(a).

Complementing this picture, we observe [Fig. 8(a) and (c), blue marks] reductions in R_S and R_D as a result of the initial high $V_{D\text{stress}}$ that remains stable as $V_{D\text{stress}}$ is reduced. The recoverable component of R_D degradation also follows a hot-electron type law [Figs. 6 and 7(b)].

In all these experiments, there was little change in I_{Goff}.

To better separate and identify the roles of $V_{D\text{stress}}$ and gate stress, we have conducted constant stress experiments under high $V_{D\text{stress}}$ and low $I_{D\text{stress}}$ condition as described in the following section.

IV. Constant Stress Experiment at High $V_{D\text{stress}}$

In order to focus on the impact of high $V_{D\text{stress}}$, we carried out a constant stress experiment at $V_{D\text{stress}} = 30$ V and $I_{D\text{stress}} = 80$ mA/mm. 80 mA/mm was chosen so that the overall power consumed would not be too high such that we limit self-heating. The device was characterized every 1 s and the total stress time was 6 min.

Fig. 9 shows the initial values and the evolution of the selected FOMs during stress as well as the final detrapped values that reflect permanent degradation. Examining the initial and final points for all the four subplots, we reach several conclusions. As a result of stress, there is a permanent increase in $I_{D\text{max}}$, a permanent small negative shift in $V_{T\text{lin}}$, permanent small reductions in R_D and R_S, and a small increase in I_{Goff}. All these changes are consistent with the observations in the constant-power-stress experiment set in the previous section (device 3).

If we focus on the evolution of FOMs during stress, we observed interesting phenomena. During the first

TABLE II

SUMMARY OF DEGRADATION OF DEVICE FOMS UNDER ELECTRICAL AND THERMAL STRESS CONDITIONS. NOT CAPTURED IN THE TABLE IS A SECOND TRAPPING MECHANISM WITH A SLOWER TIME CONSTANT THAT TAKES PLACE UNDER HIGH $V_{D\text{stress}}$ AND LOW $I_{D\text{stress}}$ CONDITIONS AND AFFECTS, AS MENTIONED IN THE TEXT, THE INTRINSIC PORTION OF THE DEVICE

	low $V_{Dstress}$, high $I_{Dstress}$		high $V_{Dstress}$, low $I_{Dstress}$		thermal
	permanent	recoverable	permanent	recoverable	permanent
I_{Dmax}	↓	–	↑	↓	↓
ΔV_T	> 0 (small)	< 0 (small)	< 0	< 0	> 0
R_D	–	↑ (small)	↓	↑	↑
R_S	–	–	↓	↓	↑
location of degradation	intrinsic device, towards drain	too small to distinguish	entire device	extrinsic device	entire device
physical origin	gate sinking	too small to distinguish	de-passivation of pre-existing defects	hot electron trapping	gate sinking

few seconds, $I_{D\text{max}}$ and R_S abruptly decrease, while R_D abruptly increases and $V_{T\text{lin}}$ quickly shifts negative. These changes are consistent with the transient observations made in the previous section (device 3). There is also a sudden increase in I_{Goff} at the beginning of the experiment.

As time evolves, $V_{T\text{lin}}$ and I_{Goff} partially recover with similar time constants while $I_{D\text{max}}$, R_D, and R_S remain relatively constant. The increased I_{Goff} and its subsequent reduction with further stress time mostly flows through the source (not shown). All this suggests that there are two separate trapping mechanisms acting in different regions with different time constants. The fast trapping mechanism that brings $I_{D\text{max}}$ down and increases R_D is likely due to the hot electron mechanism postulated above that mostly takes place on the drain side of the device. This would result in a reduction in sheet carrier concentration on the extrinsic drain that manifests itself as an increase of R_D. More significantly, there would be a prominent rise of drain resistance at high drain current as electrons approach saturated velocity in the extrinsic drain [22]. This would bring $I_{D\text{max}}$ down. A clear example of this can be seen in Fig. 3(a).

On a slower timescale, there is trapping that produces a positive V_T shift and a reduction of I_{Goff}. Since no change takes place in R_S and R_D, this mechanism seems to affect the intrinsic device most likely inside the AlN barrier or at the interface with the GaN channel.

V. DISCUSSION

From the above experiments, an overall picture of degradation emerges that is summarized in Table II. Two separate permanent degradation mechanisms plus two trapping processes are in action simultaneously.

At low and moderate $V_{D\text{stress}}$, there is a permanent reduction in $I_{D\text{max}}$, a small positive shift in V_T and a small increase in R_D with little change in R_S. This suggests degradation in the intrinsic portion of the device, perhaps toward its drain end. The permanent degradation of $I_{D\text{max}}$ and R_D increase with $V_{D\text{stress}}$ but are eventually swamped by the second mechanism. This kicks in at high $V_{D\text{stress}}$ and results in an additional permanent negative V_T shift that introduces a permanent increase in $I_{D\text{max}}$ and permanent reductions in R_S and R_D. This mechanism is consistent with an increase in electron concentration in the channel and seems to affect the entire device. Separately, there is evidence of recoverable hot-electron trapping preferentially taking place on the drain side of the device as well as a slower trapping process that is consistent with electron trapping in the barrier.

We have tried exposure under UV light with energy as high as 4.9 eV to detrap the degraded device. We have also regularly monitored the device over a period of months. None of this leads to any V_T recovery, so we believe that V_T shift is permanent.

The permanent negative V_T shift under high $V_{D\text{stress}}$ is consistent with the results reported in [23]–[25]. These papers provide evidence of depassivation of hydrogenated defects in the GaN channel as a result of collisions with energetic electrons. Under the right conditions, negatively charged defects can become neutral after the collision, leading to a negative threshold voltage shift.

At low $V_{D\text{stress}}$, $I_{D\text{stress}}$ is high and $I_{G\text{stress}}$ is also high (~87 mA/mm). In this regime, we see a small positive permanent V_T shift that results in a drop in permanent $I_{D\text{max}}$. This could be due to gate sinking. In this bias configuration, the field distribution is tightly confined to the vicinity of the gate, which is therefore expected to get very hot. This hypothesis is also consistent with the greater degree of permanent damage that we observe under these stress conditions on the drain side versus the source side. This is because the hotspot is on the drain side.

We have confirmed this hypothesis by conducting a pure thermal stress experiment on virgin devices at 400 °C in an N_2 environment. After thermal stress, permanent $I_{D\text{max}}$ was found to decrease by 29%, while permanent V_T shifted positive by 0.19 V. This is consistent with the changes induced in the low $V_{D\text{stress}}$ high $I_{D\text{stress}}$ stress regime.

Separately from all this, there is hot-electron-induced trapping, most likely in the extrinsic drain of the device. We believe this trapping mechanism to be the same as the fast trapping mechanism suggested in the constant stress experiment at high $V_{D\text{stress}}$ in Section IV. Similar recoverable increases in R_D and decreases in I_D have been reported in the literature due to hot-electron-related degradation [12], [26]–[29]. Ours is, however, the first clear observation of a hot electron-type law in this material system (Fig. 6). A second trapping mechanism taking place on a slower timescale, as reflected in Section IV, is believed to be due to electron trapping in traps inside the AlN barrier and/or at the interface with the GaN channel.

VI. CONCLUSION

We have carried out a systematic study of electrical degradation of InAlN/GaN HEMTs under ON conditions. We have identified two dominant permanent degradation mechanisms

as well as two recoverable trapping-related degradation mechanisms. Under high drain voltage with the device ON, we observe a permanent increase in I_{Dmax}, which is explained by a permanent negative shift in V_T that is attributed to dehydrogenation of preexisting defects. Under the same stress conditions, there is also a prominent but recoverable hot-electron trapping on the drain side of the device that brings $I_{D\mathrm{max}}$ down and increases R_D. A second trapping mechanism with a longer time constant also exists that shifts V_{T} positive and brings $I_{D\mathrm{max}}$ down. Under low electric field and high current stress conditions, a separate permanent degradation mechanism has emerged that is characterized by a noticeable permanent reduction in $I_{D\mathrm{max}}$ and a positive V_T shift. This is also the signature of pure thermal stress, which allows us to attribute this to gate sinking. Our study should be instrumental in enhancing the electrical reliability of InAlN/GaN HEMTs for millimeter-wave applications.

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